FORM PTO-1390 (rev. 12-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY DOCKET NUMBER: HU-5890

U.S. APPLICATION NO. (IF KNOWN): 09/913917

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/CH00/00056	02 February 2000	23 February 1999

TITLE OF INVENTION

PRINTED CIRCUIT BOARD FOR ELECTRICAL AND OPTICAL SIGNALS AND METHOD FOR PRODUCING THE SAME

APPLICANT(S) FOR DO/EO/US

STRAUB, Peter Leo

Applicant Herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 317(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371 (c)(2)).
7. ☐ Amendment to the claims of the International Application under PCT Article 19 (35 U.S.C. (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau)
   b. ☐ have been transmitted by the International Bureau
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ Have not been made and will not be made
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. (c)(3))
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. (c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording.
    A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information, as listed:

EXPRESS MAIL LABEL # EF 163 925 963 EF

DATE MAILED: 8.21.01

SIGNATURE: Kathleen McCafferty

U.S. APPLICATION NO. (if known)	INTERNATIONAL APPLICATION NO.	ATTORNEY DOCKET NO
09/913917	PCT/CH00/00056	HU-5890

17. ☒ The following fees are submitted:

	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(A)(1)-(5)):	
Search Report has been prepared by the EPO or JPO $ 860.00	
International Preliminary Examination fee paid to USPTO (37 CFR 1.482) $ 690.00	
No international preliminary examination fee paid To USPTO (37 CFR 1.482) but international search Fee paid to USPTO (37 CFR 1.445(a)(2)) $ 710.00	
Neither international preliminary fee (37 CFR 1.482) Nor international search fee (37 CFR 1.44 (a)(2) Paid to USPTO $1,000.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied Provisions of PCT Article 33 (2)-(4) $ 100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 Months from the earliest claimed priority date (37 CFR 1.492(e))	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total Claims	21 - 20		X $ 18.00	$
Independent Claims	1 - 3		X $ 80.00	$
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$
TOTAL OF ABOVE CALCULATIONS =				$ 860.00
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9,1.27,1.28).				$
SUBTOTAL =				$ 860.00
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR .492(f)).				$
TOTAL NATIONAL FEE =				$ 860.00
Fee for recording the enclosed assignment (37 CFR 1.21 (b)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28,3.31). $40.00 per property +				$
TOTAL FEES ENCLOSED =				$ 860.00
			Amount to be Refunded:	$
			Amount to be refunded:	$

a. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **20-0090**. A duplicate of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.127 (a)or(b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
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I hereby certify that this paper or fee is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington D.C. 20231

Signature Kathleen McCafferty

8.21.01
Date of Deposit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	STRAUB, P.L.
U.S. Serial No.	:	
U.S. Filing Date	:	Concurrently Herewith
International Appln No.	:	PCT/CH00/00056
International Filing Date	:	02 February 2000
Priority Date(s) Claimed	:	23 February 1999
Title	:	PRINTED CIRCUIT BOARD FOR ELECTRICAL AND OPTICAL SIGNALS AND METHOD FOR PRODUCING THE SAME
Attorney Docket No.	:	HU-5890
		Cleveland, Ohio 44114

BOX PCT
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Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination of the above-identified application, entry of the present amendment is respectfully requested.

IN THE CLAIMS

7. (Amended) A circuit board according to claim 2, characterized in that the carrier plates (10, 16) are each made of an electrically insulating material which is used as the

base material for the production of electric circuitboards, preferably an Aramid-reinforced resin.

8. (Amended) A circuitboard according to claim 1, characterized in that the thin glass layers (11, 17) have a thickness of less than or equal to 1.1 mm and are made of a borosilicate glass.

9. (Amended) A circuitboard according to claim 1, characterized in that the thin glass layers (11, 17) and the carrier plates (10, 16) are glued or pressed together.

10. (Amended) A circuitboard according to claim 1, characterized in that at least individual layers of the thin glass layers (11, 17) are designed as continuous layers.

11. (Amended) A circuitboard according to claim 1, characterized in that at least individual layers of the thin glass layers (11, 17) are structured so as to form individual optical conductors (13) within the layer, separated from one another by interspaces (12).

13. (Amended) A circuitboard according to claim 11, characterized in that the interspaces (12) between the optical conductors (13) are filled with a filling material (14, 18).

14. (Amended) A circuitboard according to claim 1, characterized in that coupling openings (26, 28) are provided for optical coupling of optically active elements (25, 27) arranged on the top and or bottom sides of the circuitboard (30), so that the concealed thin glass layer(s) (11, 17) or optical conductors (13) located in an optical conduction level (OL) are accessible from the outside through these coupling openings.

15. (Amended) A method of producing a circuitboard according to claim 1, characterized in that in a first step at least one thin glass layer (11, 17) is joined over the entire area to at least one carrier plate (10, 16) to form an optical sandwich (15; 15.1, …, 15.3), and in a second step, the optical sandwich (15; 15.1, …, 15.3) is connected to the circuitboard (30) as an optical conduction level (OL) having one or more electrical conduction levels (EL) in a stack arrangement.

17. (Amended) A method according to claim 15, characterized in that the thin glass layer (11, 17) joined to the carrier plate (10, 16) is structured between the first and second steps.

20. (Amended) A method according to claim 17, characterized in that the free surface area of the structured thin glass layer (11) is coated with a reflective layer (29), preferably made of a metal, by vapor deposition, galvanic or chemical deposition.

21. (Amended) A method according to claim 17, characterized in that the interspaces (12) in the structured thin glass layer (11, 17) are filled with a filling material (14, 18) having a refractive index lower than the refractive index of the glass of the thin glass layer (11, 17).

REMARKS

Examination of the above-identified application in view of the present amendment is respectfully requested.

The present amendment before action removes the multiple dependency appearing in the claims.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made"**.

An early action on the merits is respectfully requested. Please charge any deficiency or credit any overpayment in the fees for this matter to our Deposit Account No. 20-0090.

Respectfully submitted,

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"Version With Markings to Show Changes Made"

In the Claims:

Claims 1-6 remain unchanged.

Claim 7 has been amended, as follows:

7. (Amended) A circuit board according to ~~one of claims 2-6~~ claim 2, characterized in that the carrier plates (10, 16) are each made of an electrically insulating material which is used as the base material for the production of electric circuitboards, preferably an Aramid-reinforced resin.

Claim 8 has been amended, as follows:

8. (Amended) A circuitboard according to ~~one of claims 1-7~~ claim 1, characterized in that the thin glass layers (11, 17) have a thickness of less than or equal to 1.1 mm and are made of a borosilicate glass.

Claim 9 has been amended, as follows:

9. (Amended) A circuitboard according to ~~one of claims 1-8~~ claim 1, characterized in that the thin glass layers (11, 17) and the carrier plates (10, 16) are glued or pressed together.

Claim 10 has been amended, as follows:

10. (Amended) A circuitboard according to ~~one of claims 1-9~~ claim 1, characterized in that at least individual layers of the thin glass layers (11, 17) are designed as continuous layers.

Claim 11 has been amended, as follows:

11. (Amended) A circuitboard according to ~~one of claims 1-9~~ claim 1, characterized in that at least individual layers of the thin glass layers (11, 17) are structured so as to form individual optical conductors (13) within the layer, separated from one another by interspaces (12).

Claim 12 remains unchanged.

Claim 13 has been amended, as follows:

13. (Amended) A circuitboard according to ~~one of claims 11 and 12~~ claim 11, characterized in that the interspaces (12) between the optical conductors (13) are filled with a filling material (14, 18).

Claim 14 has been amended, as follows:

14. (Amended) A circuitboard according to ~~one of claims 1-13~~ claim 1, characterized in that coupling openings (26, 28) are provided for optical coupling of optically active elements (25, 27) arranged on the top and or bottom sides of the circuitboard (30), so that the concealed thin glass layer(s) (11, 17) or optical conductors (13) located in an optical conduction level (OL) are accessible from the outside through these coupling openings.

Claim 15 has been amended, as follows:

15. (Amended) A method of producing a circuitboard according to ~~one of claims 1 through 14~~ claim 1, characterized in that in a first step at least one thin glass layer (11, 17) is joined over the entire area to at least one carrier plate

(10, 16) to form an optical sandwich (15; 15.1, …, 15.3), and in a second step, the optical sandwich (15; 15.1, …, 15.3) is connected to the circuitboard (30) as an optical conduction level (OL) having one or more electrical conduction levels (EL) in a stack arrangement.

Claim 16 remains unchanged.

Claim 17 has been amended, as follows:

17. (Amended) A method according to ~~one of claims 15 and 16~~ claim 15, characterized in that the thin glass layer (11, 17) joined to the carrier plate (10, 16) is structured between the first and second steps.

Claim 18 remains unchanged.

Claim 19 remains unchanged.

Claim 20 has been amended, as follows:

20. (Amended) A method according to ~~one of claims 17 through 19~~ claim 17, characterized in that the free surface area of the structured thin glass layer (11) is coated with a reflective layer (29), preferably made of a metal, by vapor deposition, galvanic or chemical deposition.

Claim 21 has been amended, as follows:

21. (Amended) A method according to ~~one of claims 17 through 20~~ claim 17, characterized in that the interspaces (12) in the structured thin glass layer (11, 17) are filled with a filling material (14, 18) having a refractive index lower than the refractive index of the glass of the thin glass layer (11, 17).

DESCRIPTION 4/ pgs

PRINTED CIRCUITBOARD FOR ELECTRICAL AND OPTICAL SIGNALS AND METHOD FOR PRODUCING THE SAME

TECHNICAL BACKGROUND

The present invention relates to the field of circuitboard technology. It concerns a circuitboard having at least one electrical conduction level for relaying electric signals and/or currents and at least one optical conduction level for relaying optical signals, said conduction levels being interconnected and arranged one above the other in a stack within the printed circuitboard.

Such a circuitboard is disclosed, for example, in the publication U.S. Patent No. 5,408,568 A.

This invention also relates to a method of producing such a circuitboard.

STATE OF THE ART

In the long run, the demand for higher and higher clock rates and faster and faster signal transmission cannot be met with an adequate quality by using copper lines. Through the use of optical transmission pathways (optical fibers) it is possible to transmit signals at extremely high transmission rates within a backplane and also on system boards. A high interference immunity with respect to electromagnetic interference is a very fortunate side effect which is important especially on an electric backplane. Such a backplane is responsible, for example, for the data exchange between the individual processor cards of a multiprocessor high performance computer.

Various proposals have already been made for integrating optical data transmission pathways into multilayer circuitboards. For example, U.S. Patent No. 5,230,030 A describes an optical interface for coupling to an electronic circuit in the form of multichip modules. The individual ICs are mounted on a multilayer circuitboard consisting of layers that conduct electricity, arranged in alternation with insulating layers in the form of a stack. Channels are created in the insulating layers, which consist of an optically transparent material having a low refractive index, and are then filled with another transparent plastic having a higher refractive index. The fillings then form optical conductors which are connected to the ICs on the one hand and on the other hand are led to the edge of the stack, where they can be connected externally by means of an appropriate plug. This method of integrating optical conductors into a circuitboard is not only complicated because the circuitboard must be built up and structured layer for layer in succession, but also the quality of the optical conductors produced in this way leaves much to be desired because it is very difficult to achieve a uniform and homogeneous conductor structure when filling the channels with the optically active material.

Another proposal which is disclosed in U.S. Patent No. 5,408,568 A cited above integrates a whole-area optical layer as an intermediate layer into a multilayer circuitboard. The optical layer is coupled to the outside by means of an optical fiber with a blunt connection on one end. Chips placed on the top side of the circuitboard are connected through holes beneath the chips, extending to the optical layer. The optical layer acts as a uniform optical databus over which all chips can exchange data with each other or with the outside world. No statements are made in that publication regarding the thickness or material of this optical layer. Figure 1 of that publication illustrates the optical layer with the same thickness as the printed circuitboards between which it is arranged. Therefore, this type of design could not be suitable for circuitboards having multiple optical levels and defined optical connections between selected chips.

EXPLANATION OF THE INVENTION

Therefore, the object of this invention is to create a circuitboard for electrical and optical signals which is characterized by a high quality of the

optical connection, a flexibly adaptable and easily varied design and simple integration into known manufacturing methods for multilayer circuitboards.

This object is achieved with a circuitboard of the type defined in the preamble by the fact that the optical conduction level as a conducting element comprises at least one thin glass layer. A thin glass layer is understood to refer to a sheet-like layer of glass with a small thickness (approximately 1 mm thick or less) but at the same time a high optical quality (planarity of the surfaces) such as that used for LCD displays, solar cells or as a cover for a CCD circuit. Due to the use of such thin glass layers, it is possible to provide within the circuitboard one or more space-saving optical conduction levels of a high transmission quality which can also be structured easily as needed to implement a localized optical connection within the circuitboard,

A first preferred embodiment of the circuitboard according to this invention is characterized in that the optical conduction level is formed by an optical sandwich which comprises, in addition to the minimum of one thin glass layer, at least one carrier plate which is connected to the minimum of one thin glass layer over the surface. Due to the combination of the thin glass layer with a carrier plate, it is possible to prefabricate the resulting optical sandwich separately from the fabrication of the actual circuitboard and to adapt it in a flexible manner to the prevailing needs of the circuit (e.g. by structuring). The prefabricated optical sandwich can be introduced as an additional conduction level or layer into a traditional manufacturing process for a multilayer circuitboard without requiring any significant changes in the process management.

It is possible here for the optical sandwich to comprise at least two carrier plates with the minimum of one thin glass layer arranged between them. The thin glass layer is then completely protected for further processing. However, it is also equally possible for the optical sandwich to comprise at least two thin glass layers which are connected to the minimum of one carrier plate over the area, with either the minimum of two thin glass layers being arranged on one side of the minimum of one carrier plate and joined together over the area or the minimum of two glass layers being arranged

on opposite sides of the minimum of one carrier plate. In this way, two different optical conduction levels that can be designed separately can be integrated into the circuitboard per optical sandwich. Of course, the number of carrier plates and thin glass layers per optical sandwich can also be increased further within the scope of this invention, although this does make production more complicated.

A second preferred embodiment of the circuitboard according to this invention is characterized in that the carrier plates are made of an electrically insulating material which is used as the basic material for the production of electric circuitboards, preferably an Aramid-reinforced resin. This guarantees that the optical sandwich can be introduced especially well into the traditional manufacturing process for multilayer circuitboards.

The thin glass layers preferably have a thickness of less than or equal to 1.1 mm and are made of a borosilicate glass. Such a thin glass which is available under the brand names AF 45 and D 263 from the German company DESAG for use in LCD displays or solar cells, for example, and which is available in thicknesses between 30 µm and 1.1 mm is especially suitable as the optical conduction layer because of its high optical quality.

Essentially the thin glass layer may remain unstructured, then forming a single, continuous, cohesive optical layer. Another preferred embodiment of the circuitboard according to this invention, however, is characterized in that at least individual thin glass layers are structured in such a way as to form individual optical conductors within the layer, separated from one another by interspaces. In this way, a variety of independent optical conductors can be produced in one level and can assume different transmission functions without causing any mutual interference.

The optical properties of the individual optical conductors can be optimized either by covering the exposed surfaces of the individual optical conductors with a reflective layer or by filling the interspaces between the optical conductors with a filling material which has a lower refractive index than the refractive index of the glass of the thin glass layer in particular.

Another preferred embodiment of the circuitboard according to this

invention is characterized in that coupling openings are provided for optical coupling of optically active elements arranged on the top and/or bottom sides of the circuitboard, so that the concealed thin glass layer or optical conductors inside an optical conduction level is/are accessible from the outside.

The method according to this invention for producing a circuitboard is characterized in that in a first step, at least one thin glass layer is joined to at least one carrier plate over the entire area to form an optical sandwich, and in a second step the optical sandwich is connected to the circuitboard as an optical conduction level having one or more electrical conduction levels in a stack arrangement, with the thin glass layer and the carrier plate preferably being joined together by pressing and/or gluing.

Additional embodiments are derived from the dependent claims.

BRIEF EXPLANATION OF THE FIGURES

This invention will now be explained in greater detail below on the basis of embodiments in conjunction with the drawings, which show:

Fig. 1A-D various stages in the production of an „optical sandwich" with a structured thin glass layer according to a preferred embodiment of this invention, shown in a perspective, partially cut-away view;

Fig. 2 an alternative embodiment to Figure 1D with a thin glass layer between two carrier plates;

Fig. 3 an alternative embodiment to Figure 1D with two thin glass layers arranged one above the other on one side of the carrier plates;

Fig. 4 an alternative embodiment to Figure 1D with two thin glass layers on opposite sides of the carrier plate;

Fig. 5 an enlarged sectional diagram of the optical sandwich according to Figure 1D with the interspaces of the structured thin glass

layer filled by an optically adapted filling material;

Fig. 6 an alternative embodiment to Figure 5B with a cover over the structured thin glass layer formed by a reflective layer; and

Fig. 7 an embodiment of a circuitboard according to this invention with three optical conduction levels (sandwiches) according to Figure 2, separated from one another by two electrical conduction levels arranged between them.

METHODS OF EMBODYING THIS INVENTION

In production of the circuitboard according to this invention, individual so-called „optical sandwiches" are produced first, to form the optical conduction level in a future circuitboard. The optical sandwich is produced in several steps which are shown as an example in Figure 1A-1D, starting with a carrier plate 10 (Figure 1A), which has planer surfaces on the top and bottom sides and is made of an electrically insulating material such as that used for the production of electrical circuitboards. This ensures that the finished optical sandwich can be integrated well into existing circuitboard processes from the standpoint of its material properties. The material used for this is preferably an Aramid-reinforced resin. Such carrier plates are available under the brand name Duramid-P-Cu 115ML from the German company Isola, for example. However, any other insulation material having isotropic properties and a coefficient of expansion like that of glass can also be used. The thickness of carrier plate 10 is selected so that carrier plate 10 imparts a sufficient mechanical stability to the optical sandwich, but on the other hand does not take up an unnecessary amount of height in subsequent integration into the circuitboard.

Carrier plate 10 is then joined to a thin glass layer 11 by pressing or gluing over the entire area according to Figure 1B. The thin glass layer 11 is preferably made of a borosilicate glass and has a thickness of less than or equal to 1.1 mm (30 µm to 1.1 mm). Thin glass of this type is available under the brand names AF 45 and D 263 from the German company DESAG, for example. Thin glass AF 45 is a modified borosilicate glass

with a high BaO and Al_2O_3 content and is characterized by a low thermal expansion coefficient and a high light transmission value. Due to low tolerances and flame-polished surfaces, this type of glass is especially suitable for large-area optical applications such as LCD displays, covers for CCD elements, solar cells or the like. Thin glass D 263 is a borosilicate glass with corresponding optical properties. Both of these thin glasses are available in a thickness in the range between 30 µm to 1.1 mm.

If the optical conduction level is provided only as a common databus in the subsequent circuitboard, then an optical sandwich can be integrated directly into the circuitboard with an unstructured thin glass layer according to Figure 1B (see Figure 7). However, if individual optical conduction connections are needed between different points in the plate, the thin glass layer is then structured according to Figure 1C after creation of the optical sandwich by completely removing the thin glass layer in certain areas to form interspaces 12 between individual optical conductors 13. The individual optical conductors 13 may have different areas (as shown in Figure 1C). They may run parallel to one another and may have the same or different lengths, but they may also be bent or shaped in some other manner in as much as this is consistent with their function as an optical conductor. Interspaces 12 can be created by different techniques. A mechanical method of production by grinding or milling is conceivable, but removal by means of a laser or by chemical methods is also conceivable.

After the thin glass layer 1 has been structured, the resulting interspaces 13 are filled with a filling material 14 to complete the optical sandwich 15 (Figure 1B and Figure 5). This filling operation has the advantage that a mechanically stable planer surface is formed on the top side of thin glass layer 11. On the other hand, if filling material 14 has a refractive index lower than the refractive index of the glass of thin glass layer 11, then this filling material ensures total reflection in optical conductors 13 and thus ensures good optical conduction properties. However, the same good optical conduction properties can also be achieved if the free surfaces of the structured thin glass layer 11 or the optical conductor 13 are coated with a preferably metallic reflective layer 29 by vapor deposition or by galvanic or chemical deposition in optical sandwich 15.4, as illustrated in

Figure 6. Again in this case, the remaining interspaces may be filled subsequently with a filling material for mechanical reasons.

Instead of the optical sandwich 15 from Figure 1B composed of two layers 10 and 11, optical sandwiches comprising more than two layers may also be used. In the case of optical sandwich 15.1 from Figure 2, the thin glass layer 11 is joined to carrier plates 10 and 16 on both sides. This further increases its mechanical stability. At the same time, optical sandwich 15.1 has the circuitboard material of carrier plates 10 and 16 as the connecting surface on the top and bottom sides and therefore it can be integrated especially well into the circuitboard manufacturing process.

In the case of the optical sandwich 15.2 from Figure 3, a second structured thin glass layer 17 is arranged above the first structured thin glass layer 11 and forms a second optical conduction level and thus provides additional optical connections within the circuitboard without taking up much space. In the case of the second thin glass layer 17, the interspaces are preferably also filled by a filling material 18.

Finally, in the case of the optical sandwich 15.3 from Figure 4, a structured thin glass layer 11 and 17 is provided with interspaces filled with filling material 14 and 18 on the opposite sides of carrier plate 10, thus providing a clear separation between thin glass layers 11 and 17. It is self-evident that other combinations of thin glass layers and carrier plates are also conceivable within the scope of this invention.

The finished optical sandwiches 15 and 15.1 through 15.4 can then be combined in a stack with traditional electric circuitboards that are metallized on both sides and connected to form a finished circuitboard for optical and electrical signals. The mechanical stability of these sandwiches permits problem-free integration into the production process. One such circuitboard 30 shown as an example has three optical conduction levels and two electrical conduction levels, as illustrated in a sectional view in Figure 7. The (three) optical conduction levels OL of the circuitboard 30 are formed by three optical sandwiches 15.1 according to Figure 2. Two electrical conduction levels EL are arranged in alternation between the optical conduction levels OL, each consisting of a dielectric

layer 19 and 20 in a traditional manner, coated on both sides with a metal layer 21, 22 and 23, 24 (e.g., copper lamination). All the layers are pressed or glued together. Both the thin glass layers of optical conduction levels OL and the metal layers of electrical conduction levels EL are structured according to the requirements of circuitboard 30, where the structuring of electrical conduction levels EL is accomplished in a known manner (e.g., by etching the metal layers 21-24); structuring of metal layers 21-24 is not illustrated in Figure 7 for the sake of simplicity. Of course, through-contacts such as those known and conventionally used in the technology of multilayer circuitboards may also be provided between electrical conduction levels EL.

If optically active elements or chips 25, 27 are to be connected to each other or to optical inputs or outputs, plug connections or the like through the optical conduction levels OL, then coupling openings 26, 28 are introduced into the circuitboard 30 for optical coupling of the elements 25, 27 arranged on the top and/or bottom sides of the circuitboard 30, these coupling openings providing access from the outside to thin glass layers 11 and optical conductors 13 which are concealed and lie in an optical conduction level OL. Accordingly, purely electronic chips which are arranged on the circuitboard can be connected to electric conduction levels EL by means of through-contacts (not shown in Figure 7).

LIST OF REFERENCE NOTATION

10, 16	carrier plate
11, 17	thin glass layer
12	interspace
13	optical conductor
14, 18	filling material
15; 15.1-15.3	optical sandwich
19, 20	dielectric layer
21-24	metal layer (e.g., Cu)
25, 27	optically active element (optical chip)
26, 28	coupling opening
29	reflective layer
30	circuitboard
EL	electrical conduction level
OL	optical conduction level

CLAIMS

1. The circuitboard (30) having at least one electrical conduction level (EL) for relaying electrical signals and/or currents as well as at least one optical conduction level (OL) for relaying optical signals, said conduction levels (EL, OL) being interconnected and arranged in a stack one above the other within the circuitboard, characterized in that the optical conduction level (OL) as a conducting element comprises at least one thin glass layer (11, 17).

2. A circuitboard according to claim 1, characterized in that the optical conduction level (OL) is formed by an optical sandwich (15; 15.1, ..., 15.3) comprising, in addition to the minimum of one thin glass layer (11, 17), at least one carrier plate (10, 16) which is joined to the minimum of one thin glass layer (11, 17) over the area.

3. A circuitboard according to claim 2, characterized in that the optical sandwich (15.1) comprises at least two carrier plates (10, 16) with a minimum of one thin glass layer (11) arranged between them.

4. A circuitboard according to claim 2, characterized in that the optical sandwich (15.2, 15.3) comprises at least two thin glass layers (11, 17) which are joined over the area to the minimum of one carrier plate (10).

5. A circuitboard according to claim 4, characterized in that the minimum of two thin glass layers (11, 17) are joined together over the area and are arranged on one side of the minimum of one carrier plate (10).

6. A circuitboard according to claim 4, characterized in that the minimum of two thin glass layers (11, 17) are arranged on opposite sides of the minimum of one carrier plate (10).

7. A circuitboard according to one of claims 2-6, characterized in that the carrier plates (10, 16) are each made of an electrically insulating material which is used as the base material for the

production of electric circuitboards, preferably an Aramid-reinforced resin.

8. A circuitboard according to one of claims 1-7, characterized in that the thin glass layers (11, 17) have a thickness of less than or equal to 1.1 mm and are made of a borosilicate glass.

9. A circuitboard according to one of claims 1-8, characterized in that the thin glass layers (11, 17) and the carrier plates (10, 16) are glued or pressed together.

10. A circuitboard according to one of claims 1-9, characterized in that at least individual layers of the thin glass layers (11, 17) are designed as continuous layers.

11. A circuitboard according to one of claims 1-9, characterized in that at least individual layers of the thin glass layers (11, 17) are structured so as to form individual optical conductors (13) within the layer, separated from one another by interspaces (12).

12. A circuitboard according to claim 11, characterized in that the exposed surfaces of the individual optical conductors (13) are covered with a reflective layer (29).

13. A circuitboard according to one of claims 11 and 12, characterized in that the interspaces (12) between the optical conductors (13) are filled with a filling material (14, 18).

14. A circuitboard according to one of claims 1-13, characterized in that coupling openings (26, 28) are provided for optical coupling of optically active elements (25, 27) arranged on the top and or bottom sides of the circuitboard (30), so that the concealed thin glass layer(s) (11, 17) or optical conductors (13) located in an optical conduction level (OL) are accessible from the outside through these coupling openings.

15. A method of producing a circuitboard according to one of claims 1

through 14, characterized in that in a first step at least one thin glass layer (11, 17) is joined over the entire area to at least one carrier plate (10, 16) to form an optical sandwich (15; 15.1, ..., 15.3), and in a second step, the optical sandwich (15; 15.1, ..., 15.3) is connected to the circuitboard (30) as an optical conduction level (OL) having one or more electrical conduction levels (EL) in a stack arrangement.

16. A method according to claim 15, characterized in that the thin glass layer (11, 17) and the carrier plate (10, 16) are joined together by pressing or gluing.

17. A method according to one of claims 15 and 16, characterized in that the thin glass layer (11, 17) joined to the carrier plate (10, 16) is structured between the first and second steps.

18. A method according to claim 17, characterized in that the thin glass layer is removed in certain predetermined areas in order to structure the thin glass layer (11, 17) to form individual optical conductors (13) separated from one another by interspaces (12).

19. A method according to claim 18, characterized in that the removal of the thin glass layer (11, 17) is accomplished by means of lasers or by mechanical or chemical methods.

20. A method according to one of claims 17 through 19, characterized in that the free surface area of the structured thin glass layer (11) is coated with a reflective layer (29), preferably made of a metal, by vapor deposition, galvanic or chemical deposition.

21. A method according to one of claims 17 through 20, characterized in that the interspaces (12) in the structured thin glass layer (11, 17) are filled with a filling material (14, 18) having a refractive index lower than the refractive index of the glass of the thin glass layer (11, 17).

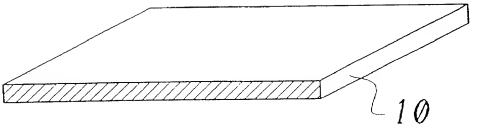

Fig. 1A

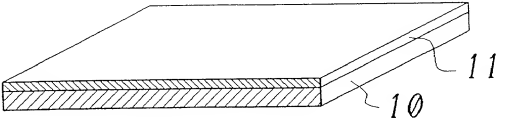

Fig. 1B

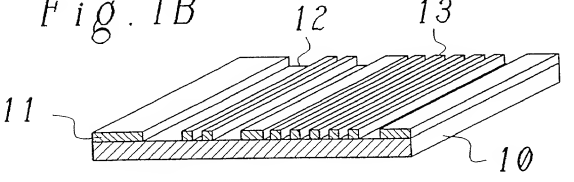

Fig. 1C

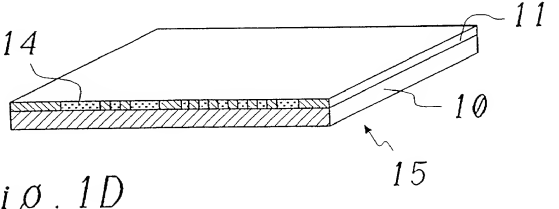

Fig. 1D

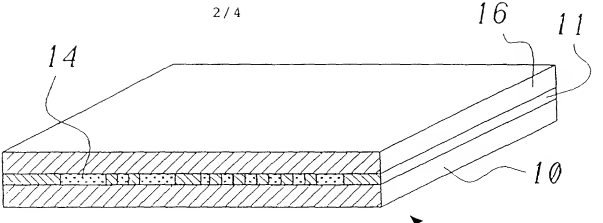

Fig. 2

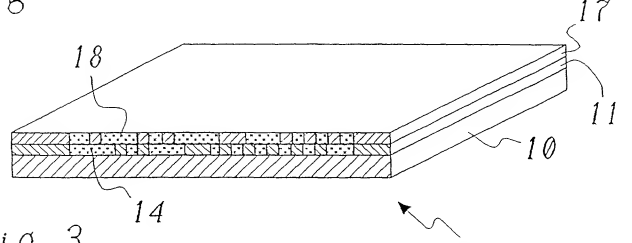

Fig. 3

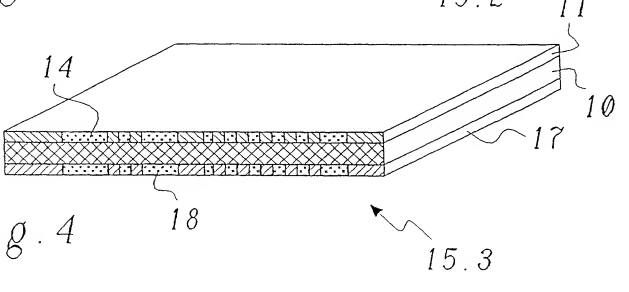

Fig. 4

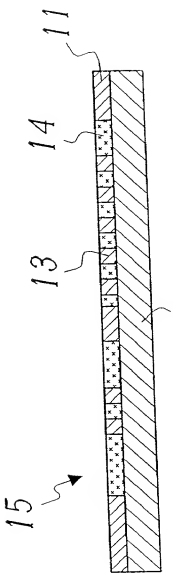

Fig. 5

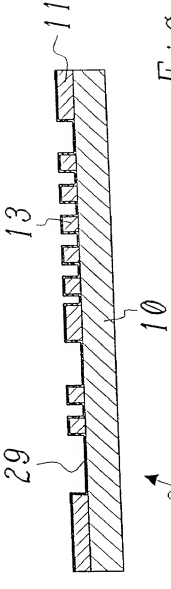

Fig. 6

15.4

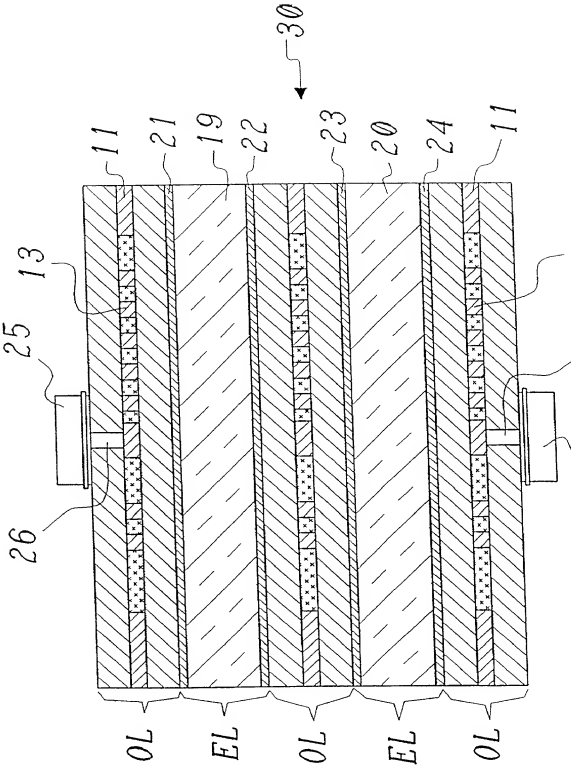

Fig. 7

Attorney Docket No. HU-5890

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PRINTED CIRCUIT BOARD FOR ELECTRICAL AND OPTICAL SIGNALS AND METHOD FOR PRODUCING THE SAME

the specification of which:

☐ is attached hereto, or

☒ was filed on 21 August 2001 as United States Application Serial No 09 / 913,917 or

☐ was filed on 02 February 2000 as International Application No. PCT/CH00/00056 and,

if known, assigned U.S. Serial No. ___/_____ on _____

for which application was amended on _____
(if applicable, by ☐ Preliminary Amendment; ☐ Article 19; ☐ Article 34).

I **HEREBY STATE** that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, §1.56.

I **HEREBY CLAIM** foreign priority benefits under Title 35, United States Code §119 or §365 of any foreign applications for patent or inventor's certificate, or §365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLN	COUNTY	FILING DATE	PRIORITY CLAIMED
CH 335/99	SWITZERLAND	23 February 1999	☒ YES ☐ NO
			☐ YES ☐ NO

I **HEREBY CLAIM** the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS (patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys: Thomas L. Tarolli, Reg. No. 20,177; Robert B. Sundheim, Reg. No. 20,127; Calvin G. Covell, Reg. No. 24,042, Barry L. Tummino, Reg. No. 29,709, Paul E. Szabo, Reg. No. 30,429; Ronald M. Kachmarik, Reg. No. 34,512, James L. Tarolli, Reg. No. 36,029; and Richard S. Wesorick, Reg. No. 40,871; each with full powers of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

SEND CORRESPONDENCE TO: **TAROLLI, SUNDHEIM, COVELL, TUMMINO & SZABO L.L.P.**
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I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and believe are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1) Full name of sole or first inventor: STRAUB, Peter Leo

Inventor's Signature _____ DATE 08/20/01

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